USB DFU requires stable levels on PA10, PB5, PB11 & PC11. PB2 must be low during boot.

R12, R13, R20 & R21 provide stable input levels for DFU.

CL = 2.2/2 + 5 (Cstray) = 6.1 pF

Reduced for reliable startup.

Clamp diode at boot pin prevents a silicon failure from short circuiting the backup battery.

Test points for JTAG debug available on bottom connector

Note: LED resistors may need to be removed for debug (Ibd).

All pins are 5V tolerant except PA4 & PA5. Therefore X skin supplier is not 5V tolerant.

PC13 is limited to 3mA out.
Note: Functions marked * are standardised symmetrical functions (except DANI**).
P86/7 and P810/11 are extra symmetrical Serial ports for F105 module.
Not available on CPUs with 2 serial ports.
Other functions may not be available with different CPUs.

Internal use ports
- PA8/DT6-VBUS
- PA10/DTG-ID
- PA11/USB-DM
- PA12/USB-OP

PC6/TX6*/PWM
PC7/RX6*/PWM
PC8/CANRXI*/PWM
PC9/CANTXI*/PWM
PC12/SS2*/CANRX2
PC13/SCK2*/CANTX2*/PWM
PC14/MSI0*/PWM
PC15/MSI2*/PWM
PC16/4k7PU*/TXD1*/PWM
PB7/SDA1*/4k7PU*/RXD1*/PWM
PC4/ADC*
PC5/ADC*
RST*
GND
3V3
VIN

1.31in x 1.65in 33mm x 42mm

DESIGN RULES.
Board profile and connector grid. 1.27mm (50mil).
Component placement grid. 0.25mm
Routing grid. 0.05mm
Minimum track and spacing. 0.15mm (6mil).
Minimum via size. Hole 0.25mm, pad 0.6mm.

PCB spec.
2 layer 1.6mm FR4. Green mask. White legend - 2 sides. Gold finish pb free. Electrical...
PYBv1.0

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