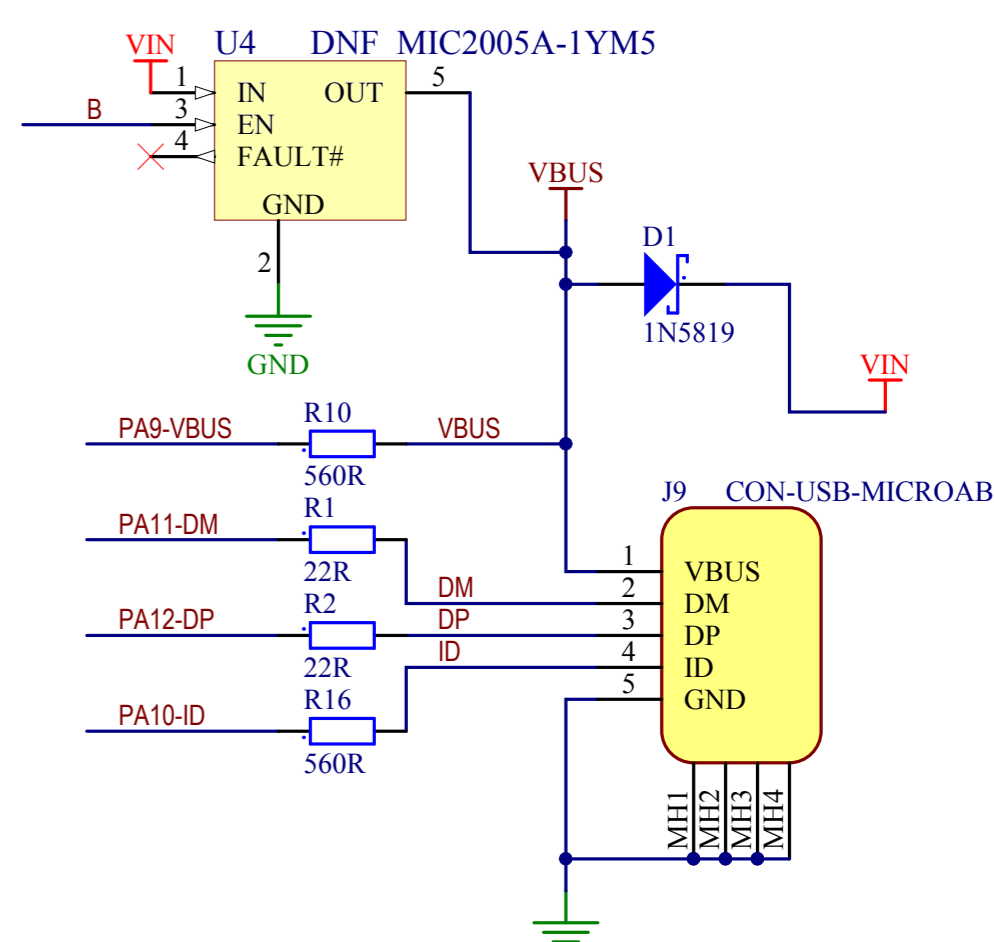
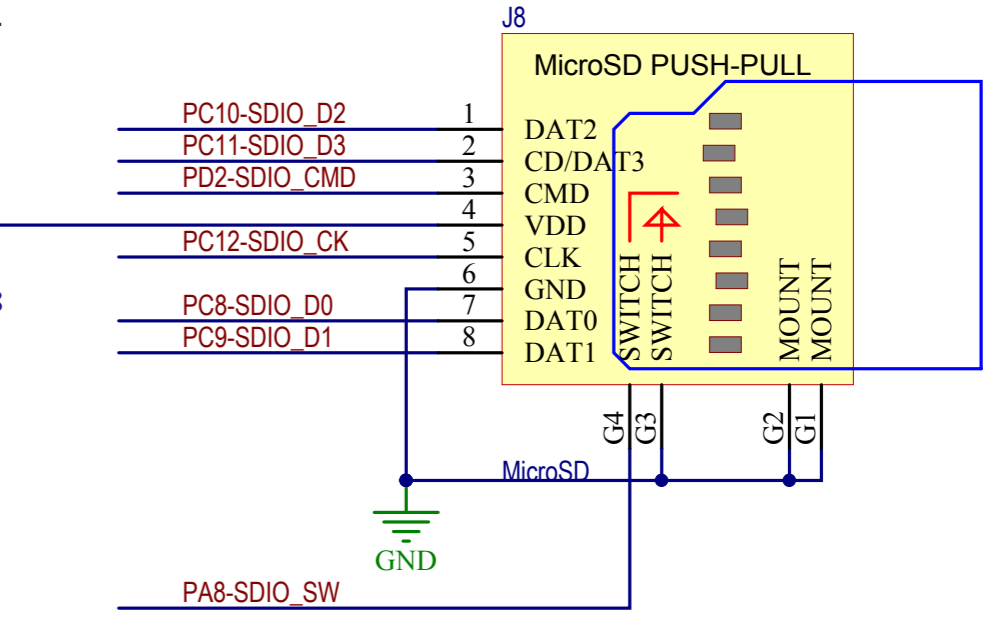
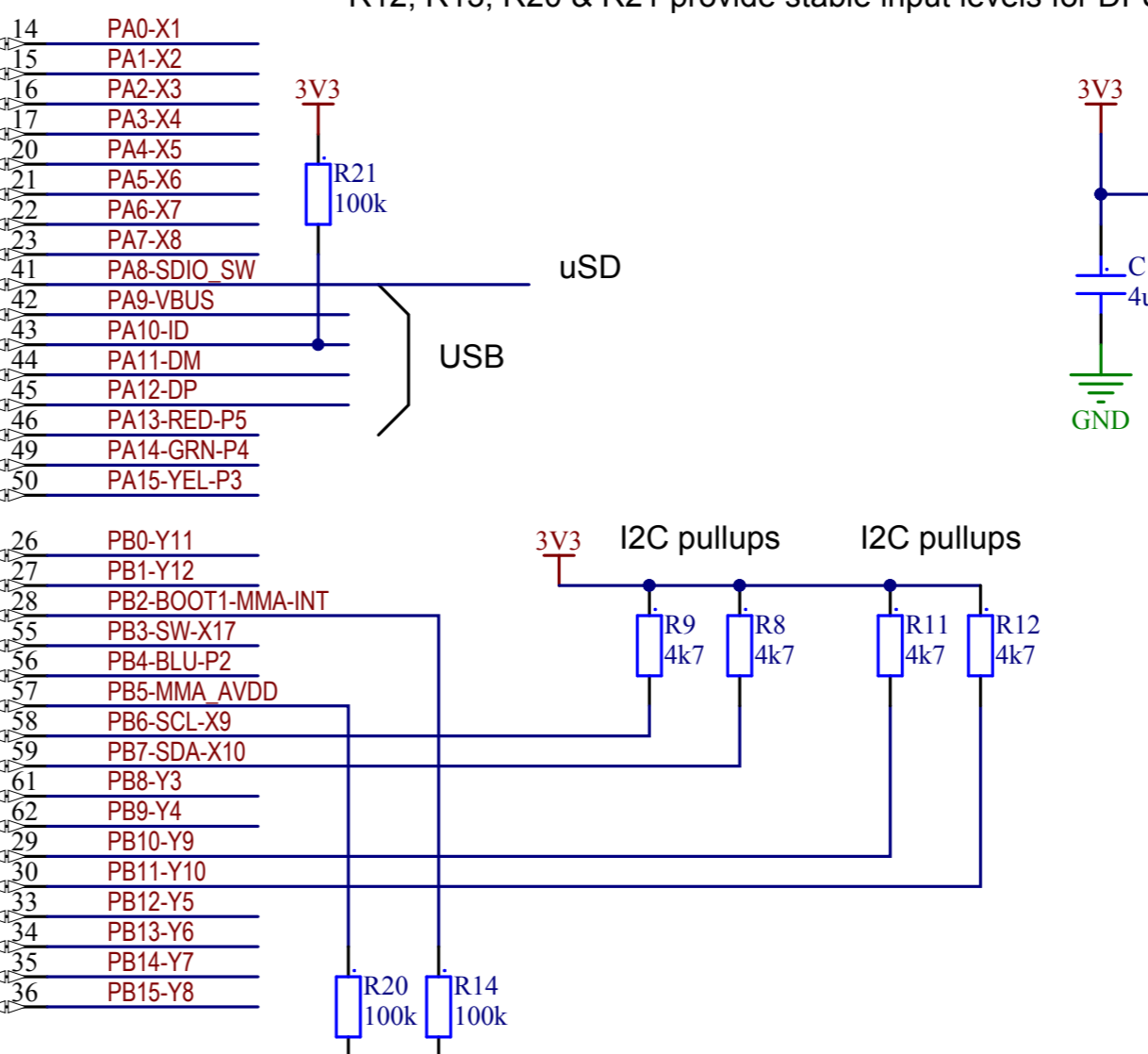
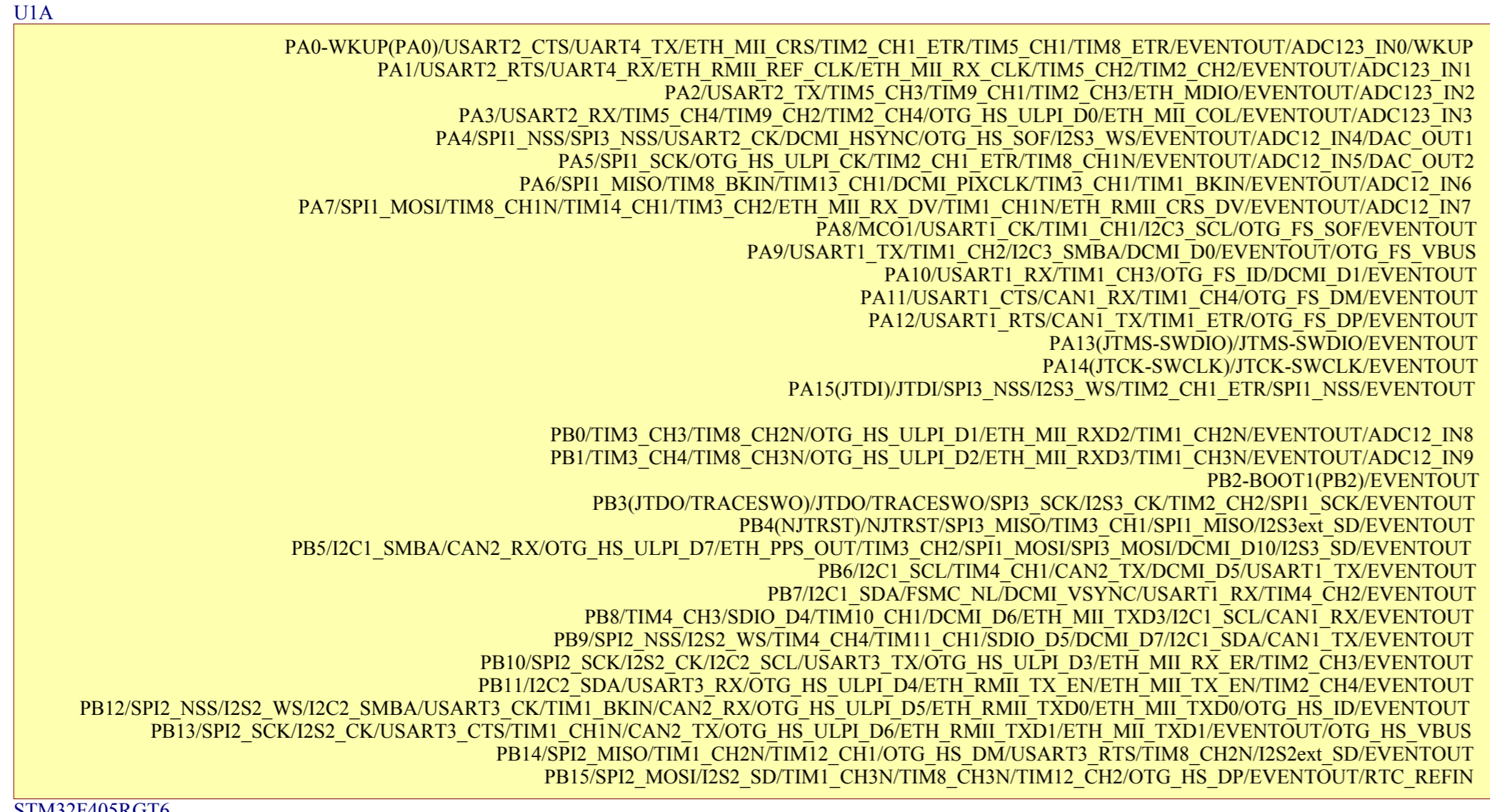
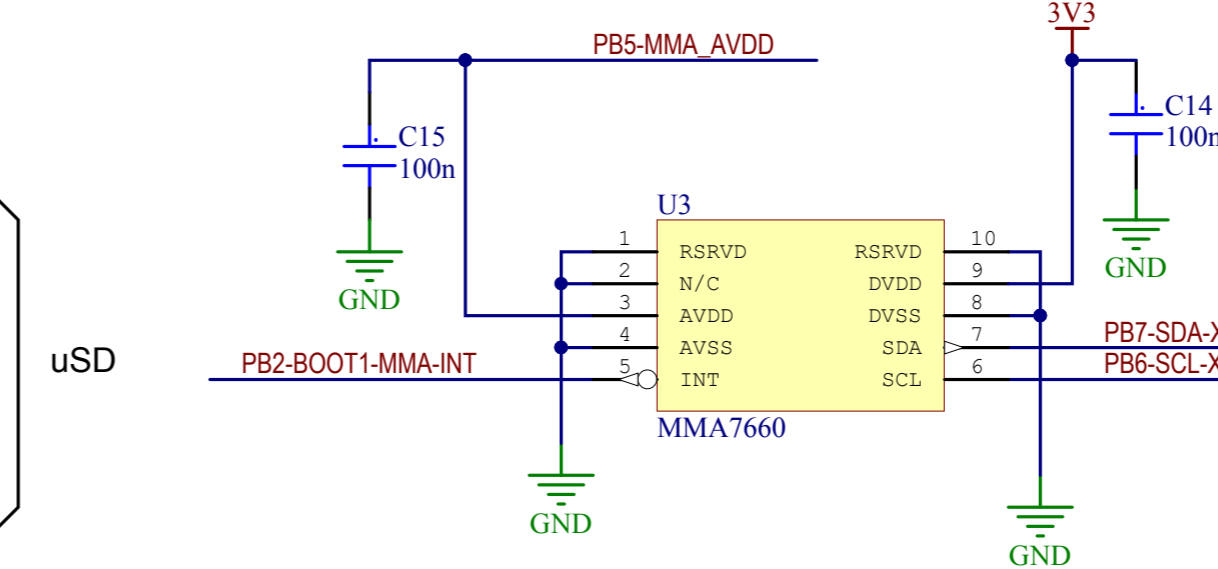
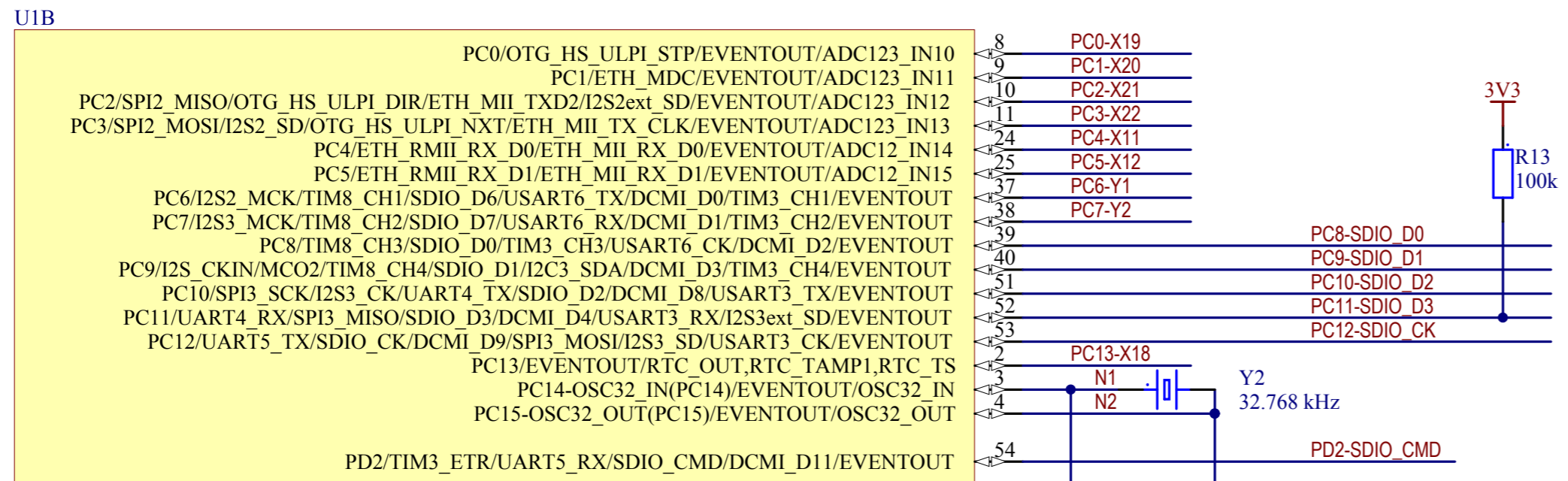


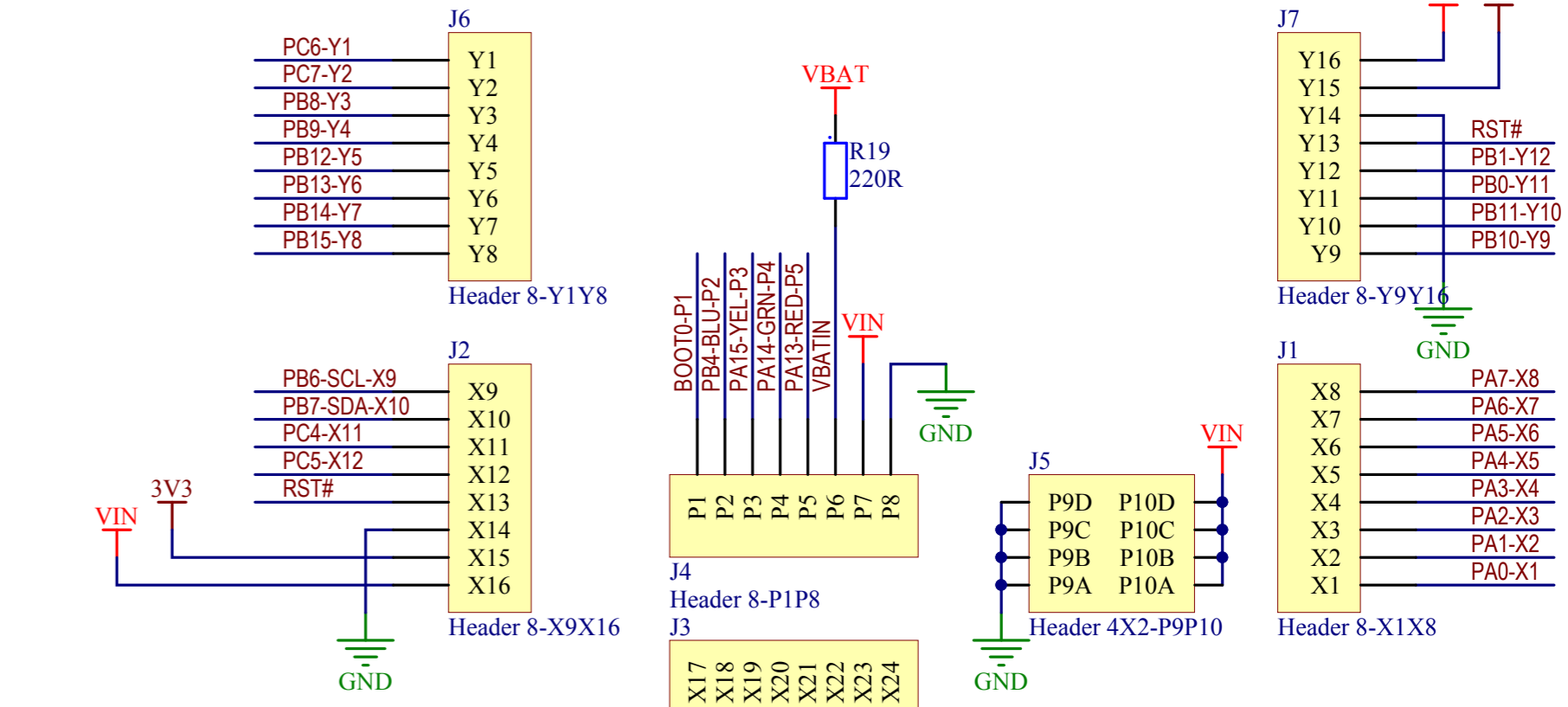
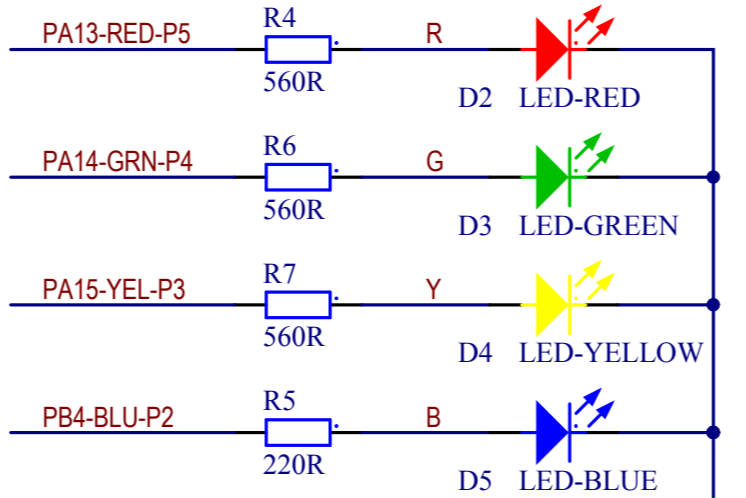
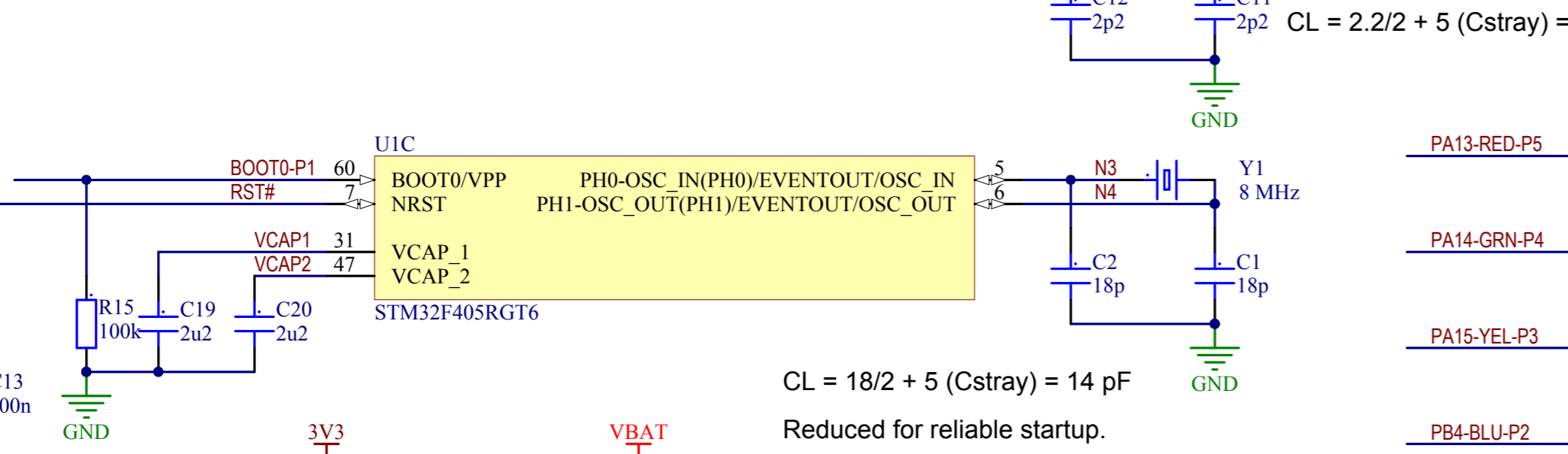
USB DFU requires stable levels on PA10, PB5, PB11 & PC11. PB2 must be low during boot.  
 R12, R13, R20 & R21 provide stable input levels for DFU.



Fit U4 for USB OTG. Vin must be 5V  
 Blue LED will indicate host mode if OTG enabled.

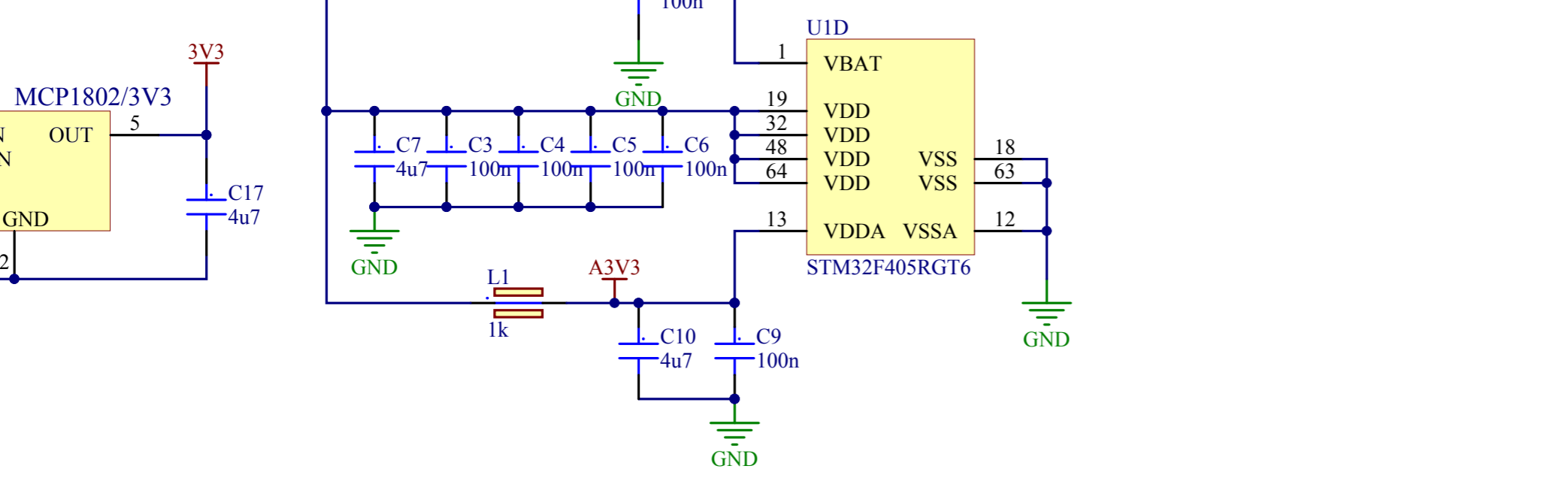


R19 prevents a silicon failure from short circuiting the backup battery.



Test points for JTAG debug available on bottom connector  
 Note: LED resistors may need to be removed for debug (tbd).

All pins are 5V tolerant except PA4 & PA5  
 Therefore X skin SPI is not 5V tolerant  
 PC13 is limited to 3mA out.



Note: Functions marked \* are standardised functions (except CAN1\*\*).

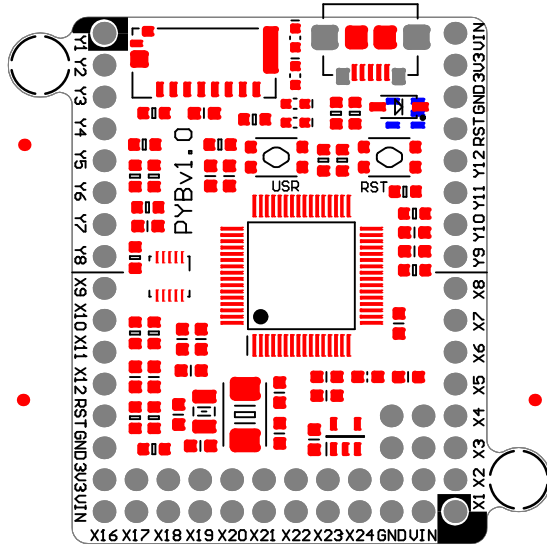
PB6/7 and PB10/11 are extra symmetrical Serial ports for F405 module.

Not available on CPUs with 2 serial ports.

Other functions may not be available with different CPUs

1.3in x 1.65in 33mm x 42mm

PC6/TX6\*/PWM\* Y1  
 PC7/RX6\*/PWM\* Y2  
 PB8/CANRX1\*\*/PWM\* Y3  
 PB9/CANTX1\*\*/PWM\* Y4  
 PB12/SS2\*/CANRX2 Y5  
 PB13/SCK2\*/CANTX2/PWM Y6  
 PB14/MISO2\*/PWM Y7  
 PB15/MOSI2\*/PWM Y8  
 PB6/SCL1\*/4k7PU/TXD1/PWM X9  
 PB7/SDA1\*/4k7PU/RXD1/PWM X10  
 PC4/ADC\* X11  
 PC5/ADC\* X12  
 RST\* X13  
 GND X14  
 3U3 X15  
 VIN X16



Y16 VIN  
 Y15 3U3  
 Y14 GND  
 Y13 RST\*  
 Y12 PB1/ADC\*/PWM  
 Y11 PB0/ADC\*/PWM  
 Y10 PB11/SDA2\*/4k7PU/RX3/PWM  
 Y9 PB10/SCL2\*/4k7PU/TX3/PWM  
 X8 PA7/MOSI1\*/ADC/PWM  
 X7 PA6/MISO1\*/ADC/PWM  
 X6 PA5/SCK1\*/ADC/DAC/PWM (3U3)  
 X5 PA4/SS1\*/ADC/DAC (3U3)  
 X4 PA3/RX2/ADC/PWM\*/SERVO  
 X3 PA2/TX2/ADC/PWM\*/SERVO  
 X2 PA1/RX4\*/ADC/PWM\*/SERVO  
 X1 PA0/TX4\*/ADC/PWM\*/SERVO

Internal use ports

PA9/OTG-VBUS  
 PA10/OTG-ID  
 PA11/USB-DM  
 PA12/USB-DP  
 PC8/SDIO\_D0  
 PC9/SDIO\_D1  
 PC10/SDIO\_D2  
 PC11/SDIO\_D3  
 PC12/SDIO\_CK  
 PA8/SDIO\_SW  
 PD2/SDIO\_CMD  
 PB6/SCL/MMA-SCL (shared with pin)  
 PB7/SDA/MMA-SDA (shared with pin)  
 PB2/BOOT1//MMA\_INT  
 PB5/MMA\_AUDD  
 PB4/BLUE\_LED/JTAG-TRST (shared with pin)  
 PA13/RED\_LED/JTAG-TMS/SWDIO (shared with pin)  
 PA14/GRN\_LED/TCK/SWCLK (shared with pin)  
 PA15/YEL\_LED/TDI (shared with pin)  
 PB3/USR\_SW/TDO/TRACESWO (shared with pin)

X17 P1  
 X18 P2  
 X19 P3  
 X20 P4  
 X21 P5  
 X22 P6  
 X23 P7  
 X24 P8  
 P9A-D  
 P10A-D

INNER ROW (P)

BOOT0	BOOT0
PB4/BLU_LED/TRST	PB4/BLU_LED/TRST
PA15/YEL_LED/TDI	PA15/YEL_LED/TDI
PA14/GRN_LED/TCK	PA14/GRN_LED/TCK
PA13/RED_LED/TMS	PA13/RED_LED/TMS
UBAT	UBAT
VIN	VIN
GND	GND
SERVO GND	SERVO GND
VIN	VIN
GND	GND
SERVO VIN	SERVO VIN
PB3/USR_SW/TDO	PB3/USR_SW/TDO
PC13(<3mA)	PC13(<3mA)
PC0/ADC	PC0/ADC
PC1/ADC	PC1/ADC
PC2/ADC	PC2/ADC
PC3/ADC	PC3/ADC
A3U3	A3U3
AGND	AGND

OUTER ROW (X)

DESIGN RULES.

Board profile and connector grid. 1.27mm (50mil).

Component placement grid. 0.25mm

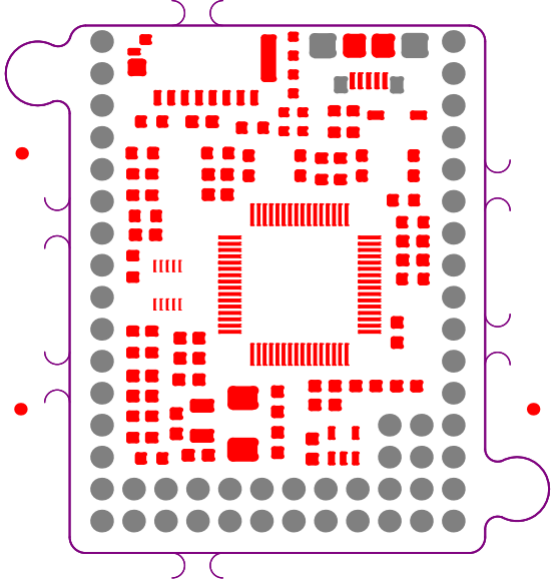
Routing grid. 0.05mm

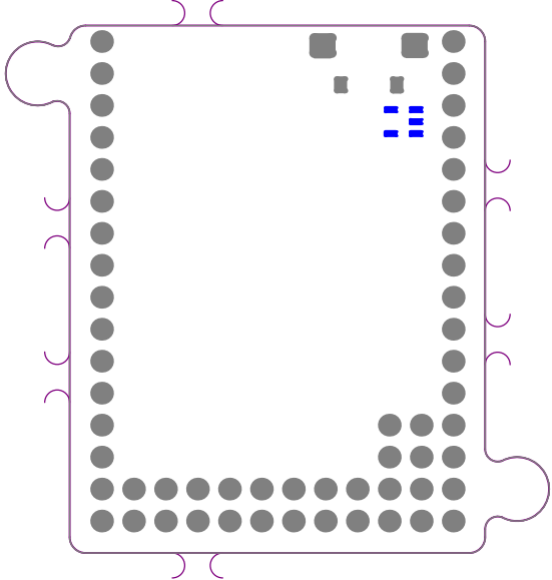
Minimum track and spacing. 0.15mm (6mil).

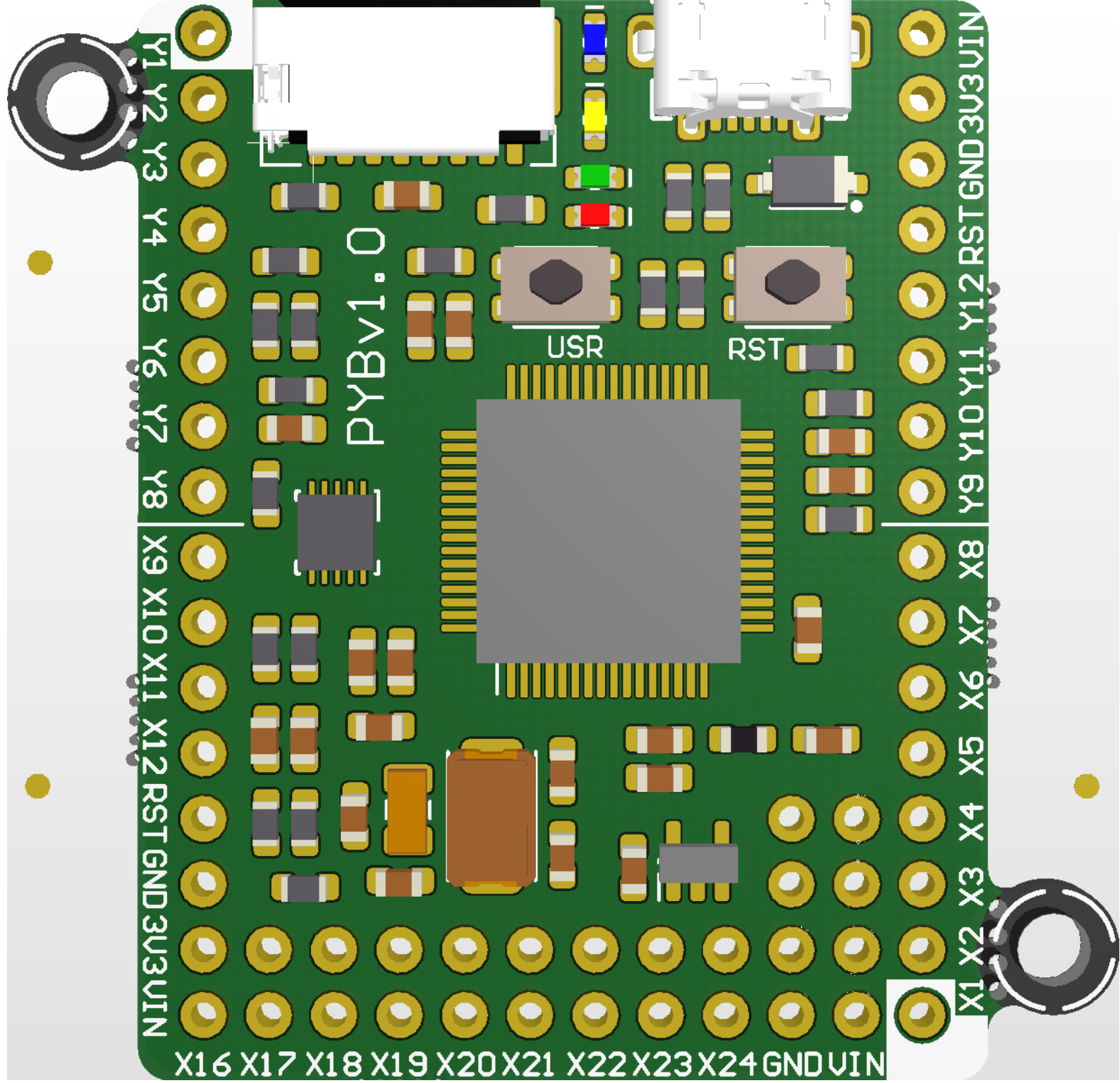
Minimum via size. Hole 0.25mm, pad 0.6mm.

PCB spec.

2 layer 1.6mm FR4. Green mask. White legend - 2 sides. Gold finish pb free. Electrical te







X16 X17 X18 X19 X20 X21 X22 X23 X24 GND VIN

X9 X10 X11 X12 RST GND 3V VIN

Y8

Y7

Y6

Y5

Y4

Y3

Y2

Y1

X1

X2

X3

X4

X5

X6

X7

X8

Y9

Y10

Y11

Y12

RST

GND

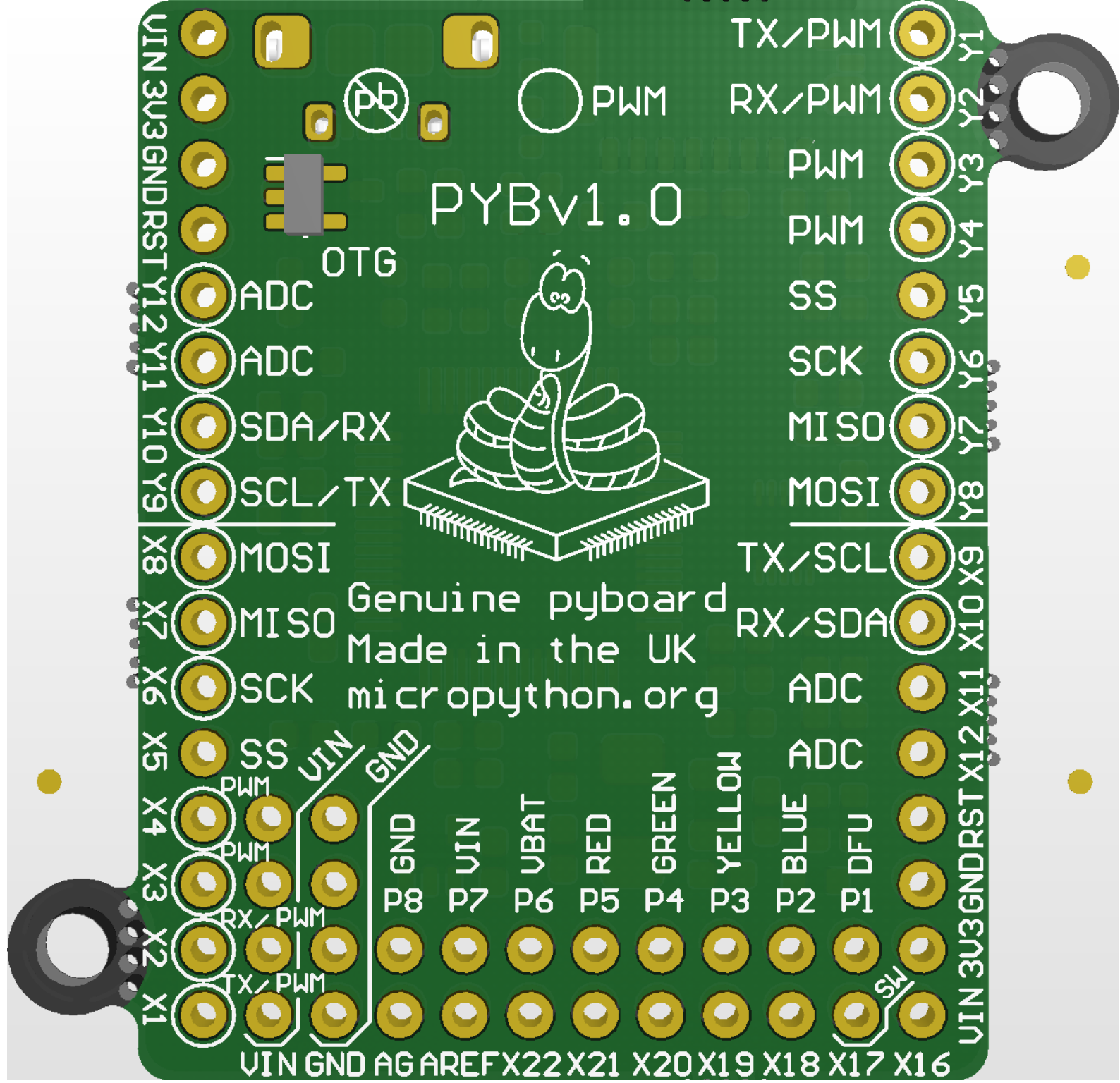
3V

VIN

RST

USR

PYBV1.0

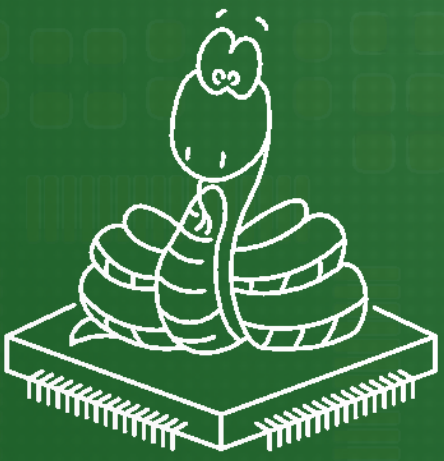


VIN 3U3GND RST Y12 Y11 Y10 Y9 X8 X7 X6 X5 X4 X3 X2 X1

ADC ADC SDA/RX SCL/TX MOSI MISO SCK SS PWM PWM RX/PWM TX/PWM

OTG VIN GND P8 P7 P6 P5 P4 P3 P2 P1 MS

PYBV1.0



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PWM

TX/PWM RX/PWM PWM PWM SS SCK MISO MOSI TX/SCL RX/SDA ADC ADC VIN 3U3GND RST X12 X11 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1

VIN GND AG AREF X22 X21 X20 X19 X18 X17 X16